AMENDMENTS TO THE CLAIMS

The following is a complete, marked up listing of the claims with underlined text indicating insertions, strikethrough and/or double-bracketed text indicating deletions, and a parenthetical indicator reflecting the status of each of the listed claims.

LISTING OF CLAIMS

1. (ORIGINAL) A semiconductor package, comprising:

a board having an upper surface, a lower surface and an aperture;

a plurality of solder bump pads formed on the lower surface of the board;

a plurality of board pads formed on the lower surface of the board;

a plurality of distribution patterns for electrically connecting the solder bump pads to the board pads;

a plurality of contact pads formed on the upper surface of the board, and electrically connected to the solder bump pads;

at least one chip having a plurality of bonding pads, disposed in the aperture;

a plurality of bonding wires electrically connecting the bonding pads to the board pads, at least one end of the bonding wires being bonded to the bonding pads or the board pads by wedge bonding;

an encapsulation part provided on the lower surface of the board for encapsulating the at least one chip, the plurality of bonding wires and the plurality of board pads; and

a plurality of solder bumps formed on the plurality of solder bump pads.

2. (ORIGINAL) The semiconductor package according to claim 1,

wherein the height of each solder bump is greater than the height of the encapsulation part extending over the lower surface of the board.

3. (ORIGINAL) The semiconductor package according to claim 1,

wherein the board is covered with a solder resist except for the regions above the plurality of solder bump pads, the plurality of contact pads and the plurality of board pads.

4. (ORIGINAL) The semiconductor package according to claim 1, further comprising:

a plurality of via holes formed through the board for electrically connecting the solder bump pads to the contact pads.

5. (ORIGINAL) A package stack including a plurality of the semiconductor packages according to claim 1,

wherein at least one solder bump of an upper package of any two adjacent packages is electrically connected to at least one contact pad of the lower package of the two adjacent packages.

6. (CURRENTLY AMENDED) A method of manufacturing a semiconductor package, comprising:

forming a plurality of solder bump pads on one surface of a board;

forming a plurality of board pads on the one surface of the board;

placing at least one chip having a plurality of bonding pads in an aperture of the board;

forming a plurality of contact pads on a surface of the board opposite the one surface of the board, the plurality of contact pads being electrically connected to corresponding ones of the plurality of solder bump pads;

wedge bonding at least one end of a plurality of bonding wires to electrically connect the bonding pads to the plurality of board pads;

encapsulating the at least one chip, the plurality of bonding wires and the plurality of board pads on the one surface of the board; and

forming a plurality of solder bumps on the plurality of solder bump pads.

7. (ORIGINAL) The method of claim 6,

wherein the height of each solder bump is greater than the height of the encapsulation part extending over the one surface of the board.

8. (ORIGINAL) The method of claim 6, wherein at least one solder bump of an upper package of any two adjacent packages is electrically connected to at least one contact pad of the lower package of the two adjacent packages.

9. (ORIGINAL) The method of claim 6, wherein the semiconductor package includes

the board having an upper surface, a lower surface and the aperture;

the plurality of solder bump pads formed on the lower surface of the board;

the plurality of board pads formed on the lower surface of the board;

the plurality of distribution patterns for electrically connecting the solder bump pads to the board pads;

the plurality of contact pads formed on the upper surface of the board, and electrically connected to the solder bump pads;

the at least one chip having the plurality of bonding pads, disposed in the aperture;

the plurality of bonding wires electrically connecting the bonding pads to the board pads;

the encapsulation part provided on the lower surface of the board for encapsulating the at least one chip, the plurality of bonding wires and the plurality of board pads; and

the plurality of solder bumps formed on the plurality of solder bump pads.

10. (NEW) A method of manufacturing a semiconductor package, comprising:

forming a board having an upper surface, a lower surface and an aperture;

forming a plurality of solder bump pads on the lower surface of the board;

forming a plurality of board pads on the lower surface of the board;

placing a semiconductor chip in the aperture, the semiconductor chip having a plurality of bonding pads arrayed on an active surface and the aperture being sized to expose substantially all of the active surface;

forming a plurality of contact pads on the upper surface of the board, the contact pads being electrically connected to corresponding ones of the solder bump pads;

wedge bonding at least one end of a plurality of bonding wires to electrically connect the bonding pads to the plurality of board pads;

encapsulating the active surface of semiconductor chip, the bonding pads, the bonding wires and the board pads; and

forming a plurality of solder bumps on the plurality of solder bump pads.

11. (NEW) A method of manufacturing a semiconductor package according to claim 10, wherein:

the bonding pads are arranged in a double row configuration.

12. (NEW) A method of manufacturing a semiconductor package according to claim 11, wherein:

each of the rows of bonding pads are positioned in peripheral regions of the active surface.

13. (NEW) A method of manufacturing a semiconductor package according to claim 10, further comprising:

forming a plurality of connective vias through the board to provide electrical contact between the contact pads and the corresponding ones of the solder bump pads.

14. (NEW) A method of manufacturing a semiconductor package according to claim 10, further comprising:

forming an insulating layer on a peripheral portion of the lower surface of the board;

wherein the bonding wires are configured to remain below a plane defined by an exposed surface of the insulating layer.

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REMARKS

No claims having been cancelled, claim 6 having been amended, and new claims 10-14 having been added, the Applicants respectfully contend that claims 1-14 are properly under consideration in this application. The above listing of the claims shows all currently active claims and their status. Entry of the amendments and reconsideration of the application in light of the amendments and the following remarks are respectfully requested.

The Applicants note with appreciation the Examiner's indication that all of the certified copies of the priority documents have been received.

Rejections under 35 U.S.C. § 102(b)

Claims 6 and 7 stand rejected as anticipated by Akram et al.'s U.S. Patent No. 5,674,785 ("Akram"). The Applicants respectfully submit that this rejection is rendered moot by the amendment reflected above to claim 6.

As noted in the Action, the cited prior art does not disclose or fairly suggest, either singly or in combination, a semiconductor device or a method of making such a semiconductor device that includes a plurality of contact pads formed on the upper face of the board, and electrically connected to the solder bump pads; at least one chip having a plurality of bonding pads, disposed in the aperture; a plurality of bonding wires electrically connecting the bonding pads to the board pads, at least one end of the bonding wires being bonded to the bonding pads or the board pads by wedge bonding; an encapsulation part provided on the lower surface of the board for encapsulating the at least one chip, the plurality of bonding wires and the plurality of board pads; and a plurality of solder bumps formed on the plurality of solder bump pads. Action at 3.

The Applicants respectfully contend that the amendment to claim 6 reflected above requires the presence of a plurality of contact pads formed on the upper surface of the board and electrically connected to the solder bump pads formed on the lower surface of the board and thus distinguishes the claim over the cited prior art. The Applicants

respectfully submit, therefore, that claim 6, and each of the claims that depend therefrom, claims 7-9, are now in condition for allowance.

New Claims 10-14

The Applicants respectfully contend that new claims 10-14 further define a method of manufacturing of a semiconductor device generally along the lines of claim 6 while introducing claim language directed to specific structural features reflected in FIGS. 1-3 of the present application. The Applicants respectfully contend that claims 10-14, like claims 6-9, are allowable over the cited references. In particular, the Applicants note that, unlike Akram, the method of claims 10-14 requires that the aperture exposes substantially all of the active surface of the semiconductor chip, rather than small central or peripheral regions. Akram's FIGS. 1 and 1A respectively. Further, claim 13 provides for the formation of conductive vias between the upper and lower surfaces of the board and claim 14 provides for bonding wires configured in a manner that excludes the conventional arching structure as illustrated throughout Akram's figures. The Applicants respectfully contend, therefore, that claims 10-14 are allowable over the cited prior art references.

Allowable Subject Matter

The Applicants note with appreciation the Examiner's indication that claims 1-5 are allowed as originally presented and that claims 8 and 9 were allowable if rewritten to remove their dependence from a rejected base claim. As detailed above, however, the Applicants respectfully submit that in light of the amendment to claim 6 indicated above, this claim is now allowable and the objections to claims 8 and 9 should be withdrawn accordingly.

CONCLUSION

In view of the above remarks and amendments, the Applicants respectfully submit that rejections have been addressed and overcome, leaving the present application in condition for allowance. A Notice to that effect is respectfully requested.

If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to contact the undersigned.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge any underpayment or non-payment of any fees required under 37 C.F.R. §§ 1.16 or 1.17, or credit any overpayment of such fees, to Deposit Account No. 08-0750, including, in particular, extension of time fees.

Very truly yours,

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